REMARKS

The specification has been amended to correct minor errors. A marked up version of the amended paragraphs of the specification is attached hereto pursuant to 37 C.F.R. § 1.121(b)(iii). Claims 1-6 have been amended for clarity. A marked up version of the amended claims is also attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). New claims 7-15 have been added. Thus, claims 1-15 are presently pending in this application for consideration.

The amendments to the present application are made to place the application in better form and to place the application in condition for allowance. No new matter has been added. Entry and consideration of these amendments prior to the first Office Action are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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Version with markings to show changes made:

IN THE SPECIFICATION:

Please amend the paragraph on page 1, starting at line 16 as follows:

The information charges are then converted into an image signal, which is a voltage signal and which is supplied, as an input, to an output amplifier 8. The output amplifier 8 is a source follower amplifier circuit in which a transistor is used for the load of a source and which, in this case, [comprises] includes interconnected three-stage source followers. Each source follower circuit is connected between a power source V_D and ground GND. An output signal from the floating diffusing layer 6, or a source follower output at the previous stage, is input to a gate of each of transistors T_{D1}, T_{D2}, T_{D3} for amplification. To a source of each of the transistors T_{D1}, T_{D2}, T_{D3}, a drain of each of load transistors T_{L1}, T_{L2}, T_{L3} is connected. These load transistors function as a constant current source for supplying a constant current between the source and the drain in accordance with a prescribed gate bias voltage.

Please amend the paragraph on page 7, starting at line 16 as follows:

These and other [objects] advantages of the invention will be explained in the description below, in connection with the accompanying drawings, in which:

IN THE CLAIMS:

Please amend the claims as indicated below:

1. (Once Amended) A charge transfer device [comprising a charge transfer section for transferring information charges in packet units, an output section provided on the output side of said charge transfer section for converting, in packet units, said information charges into a voltage signal,

and] having a source follower amplification circuit [for extracting a voltage signal subjected to impedance conversion obtained by said output section],

wherein [said] the source follower amplification circuit comprises:

an amplification transistor which receives, at a gate, [the] a voltage signal from [said] an output section and outputs, from a source, an output signal corresponding to a change in the voltage signal;

a load transistor connected between [said] the amplification transistor and a first power source for causing a constant current to flow from [said] the amplification transistor to the side of the first power source; and

a control transistor connected between [said] the amplification transistor and a second power source, wherein [said] the control transistor [cuts off] controls a current flowing from the second power source to [said] the amplification transistor according to a control signal.

2. (Once Amended) [A] The charge transfer device according to claim 1, further comprising [wherein said device comprises] an input terminal which is commonly connected to a gate of [said] the control transistor and to a gate of [said] the load transistor [commonly].

3. (Once Amended) [A] The charge transfer device according to claim 2, further comprising [wherein said device comprises] a control signal generating circuit provided between the gate of [said] the control transistor and [said] the input terminal for generating [said] the control signal based on an input signal externally input to [said] the input terminal, and [said] the load transistor maintains an on state with regard to [said] the input signal.

4. (Once Amended) [A] The charge transfer device according to claim 1, wherein [said] the control transistor is of an enhancement type.

5. (Once Amended) [A] The charge transfer device according to claim 4, further comprising [wherein said device comprises] an input terminal which is commonly connected to a gate of [said] the control transistor and to a gate of [said] the load transistor.

6. (Once Amended) [A] The charge transfer device according to claim 5, further comprising [wherein said device comprises] a control signal generating circuit provided between the gate of [said] the control transistor and [said] the input terminal for generating [said] the control signal based on an input signal externally input to [said] the input terminal, and [said] the load transistor maintains an on state with regard to [said] the input signal.